M2058/M2059 Series
SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

FEATURES

LVPECL/LVDS Differential Output
RMS Phase Jitter < 100 fs, 12 kHz to 20 MHz (156.25 MHz, PECL output)
Low Phase Noise
3rd Overtone crystal technology
Compliant to RoHS directive

APPLICATIONS

10 Gigabit Ethernet switches/routers
Network Interface

Ordering Information:

Product Family (Supply Voltage Option)	Temperature Range		Stability *		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
M2058 (3.3V) **M2059** (2.5V)	**2** **6**	-40 °C to +85 °C -20 °C to +70 °C	**3** **4** **6** **8**	±100 ppm ±50 ppm ±25 ppm ±20 ppm	**B** **U** **S**	Enable High (pad 1) No Enable/Disable Enable High (pad 2)	**P** **L**	LVPECL LVDS	**N**	Leadless	XXX.XXXX MHz
Example: M206024BPN 156.2500 MHz											
M2058	**2**		**4**		**B**		**P**		**N**		**156.2500 MHz**

- Stability includes initial tolerance @ +25°C, deviation over operating temperature, variations to supply voltage, load, vibration and shock.

LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	25		220	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1st year
RF Output						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (Vcc-2.0) V_{DC}			V	
Symmetry (duty cycle)	V_{OH}	45		55	%	Ref. to 50% of waveform
Logic Level "1"	V_{OH}	V_{cc}-1.025		V_{cc}-0.880	V	
Logic Level "0"	T_{DC}	V_{cc}-1.810		V_{cc}-1.620	V	
Rise/Fall Time	T_R/T_F		0.2	0.4	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic		70% V_{CC} or N/C			V	Pad 1 or Pad 2: Output Enabled
Disable Logic				30% V_{CC}	V	Pad 1 or Pad 2: Output Disabled to high-Z
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	
Supply Current	I_{CC}			75	mA	
Other Parameters						
Phase Jitter (RMS)	ΦJ			0.100	ps	12 KHz to 20 MHz 156.25 MHz

Revision 1
06/10/15

MtronPTI ...when timing matters

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LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	25		220	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1st year
RF Output						
Output Type		LVDS Compatible				
Output Load		100 Ω Differential			V	
Symmetry (duty cycle)	V_{OH}	45		55	%	Ref. to 50% of waveform
Differential Output Voltage	V_{DIFF}	250	350	450	mV	peak-to-peak differential output voltage
Output Offset Voltage	V_{OS}	1.125	1.250	1.375	V	
Rise/Fall Time	T_R/T_F		0.2	0.4	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic		70% V_{CC} or N/C			V	Pad 1 or Pad 2: Output Enabled
Disable Logic				30% V_{CC}	V	Pad 1 or Pad 2: Output Disabled to high-Z
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	
Supply Current	I_{CC}			40	mA	
Other Parameters						
Phase Jitter (RMS)	ΦJ			0.150	ps	12 KHz to 20 MHz 156.25 MHz

Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Vibration	Per MIL-STD-202, Method 204D, Condition D
Aging	+85°C ±3°C, 720H (No BIAS)
Humidity	+40°C ±2°CX90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1011, Condition A
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 µm maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.

...when timing matters

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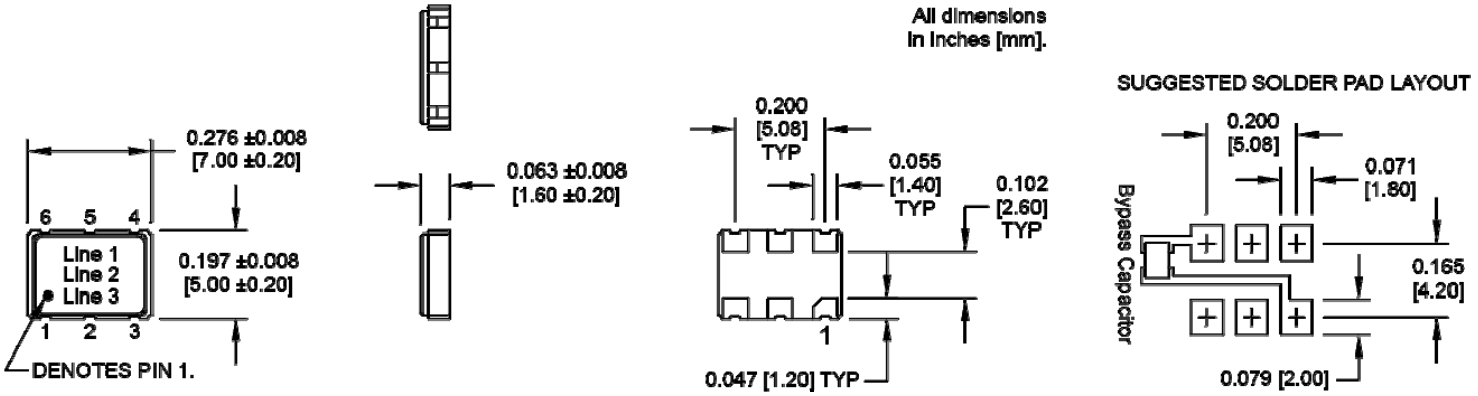
Marking, Pin Out:

Pad	Function
1	Enable/Disable or N/C
2	Enable/Disable or N/C
3	Ground
4	Output
5	Complementary Output
6	$+V_{CC}$

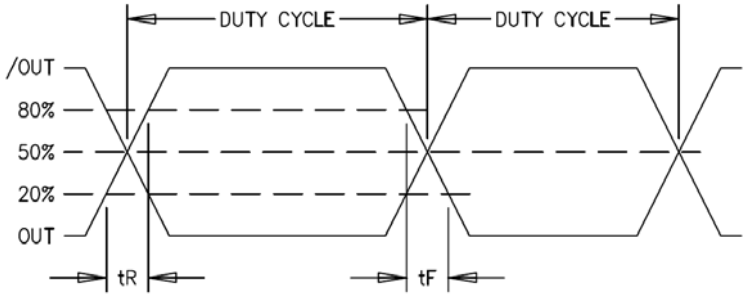
Part Marking	
Line 1	M2058/M2059
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

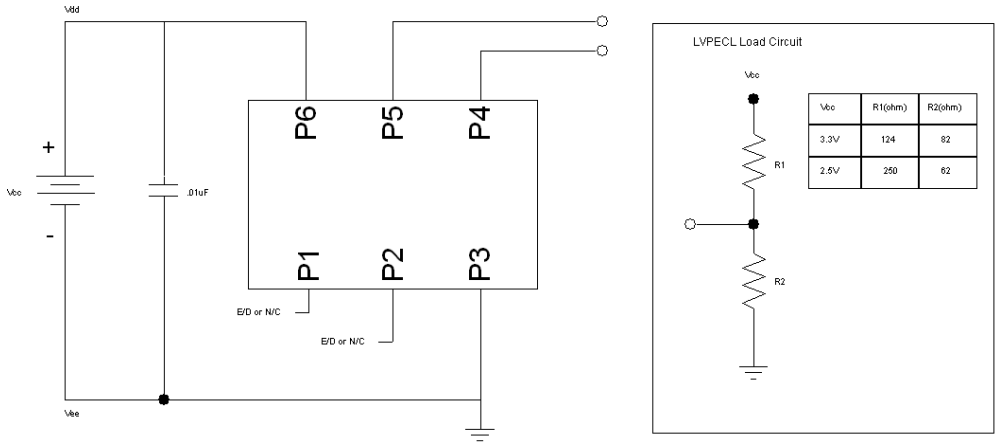
Dimensions:



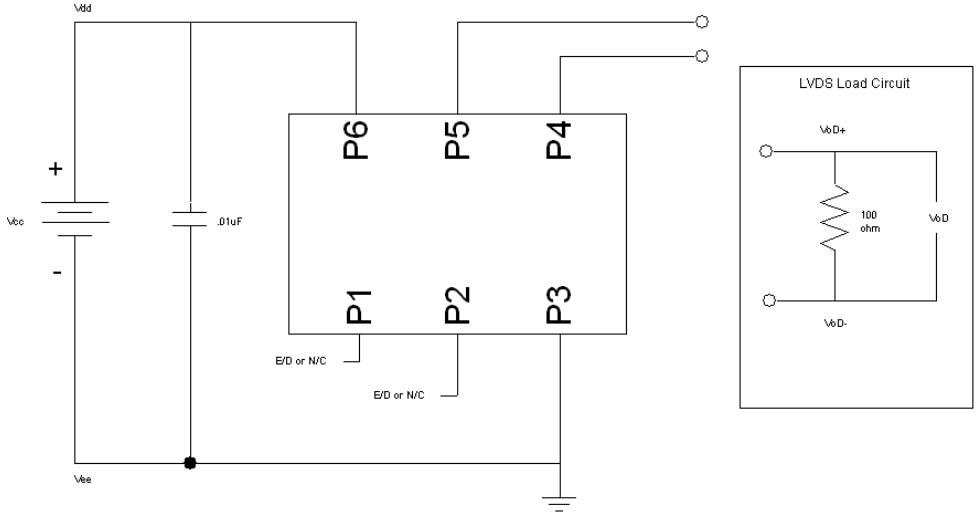
Output Waveform:



Typical LVPECL Test Circuit & Load Circuit Diagrams:



Typical LVDS Test Circuit & Load Circuit Diagrams:



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Soldering Conditions:

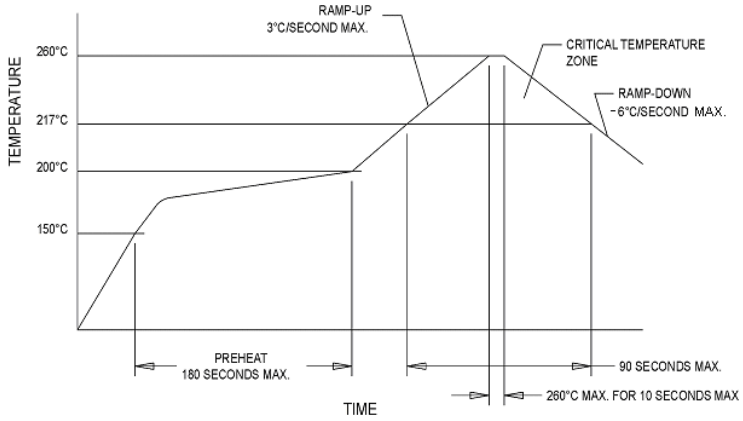
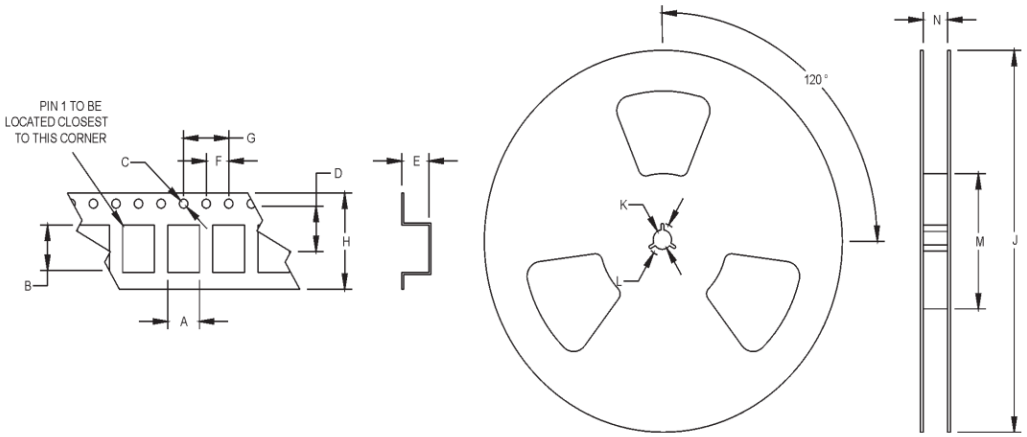


Figure 1

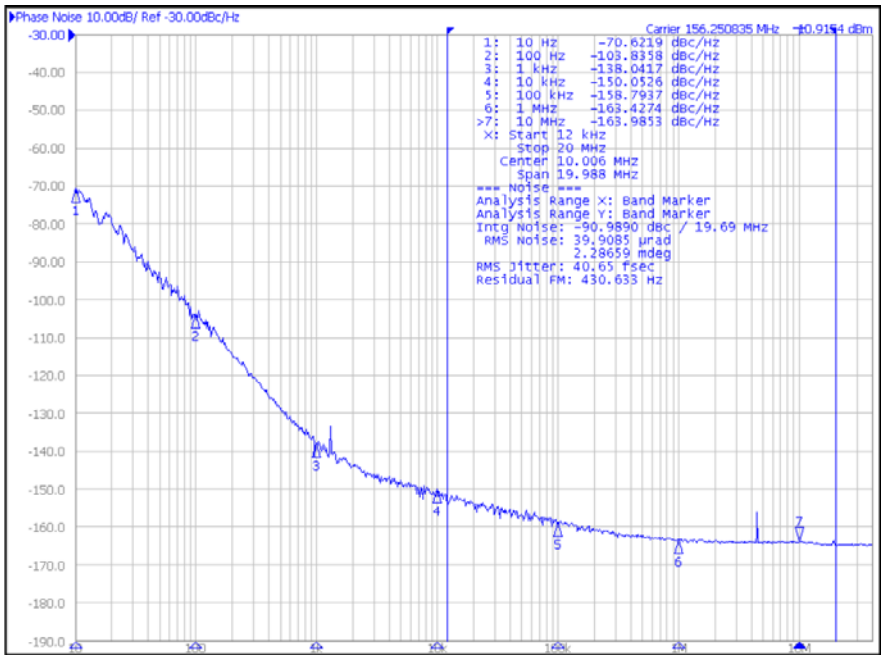
Tape and Reel Specifications:

All units in mm



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80

LVPECL Phase Noise Plot:



LVDS Phase Noise Plot: