M630x Series
5x7 mm, TCXO/TCVCXO

FEATURES

Frequencies from 10 MHz to 1.4 GHz
Supports both TCXO and VCTCXO formats
RF Output: LVPECL/LVDS/CML/CMOS
Tight stability ±1ppm over -40°C to +85°C
Wide operating temperature option available, -55°C to +105°C
Low phase noise
Operating Voltage: 1.8/2.5/3.3 V

APPLICATIONS

Telecom / Datacom
Industrial Controls
Communications & Navigation

ORDERING INFORMATION

M630x	2	J	B	V	P	C	00.0000 MHz

Product Series
M6300 = 3.3 V
M6301 = 2.5 V
M6302 = 1.8 V

Temperature Range
1: 0°C to +70°C
6: -20°C to +70°C
2: -40°C to +85°C
3: -55°C to +105°C
4: -55°C to +125°C

Stability
G: ± 0.5 ppm
H: ± 2.5 ppm
J: ± 1.0 ppm
L: ± 4.6 ppm
K: ± 2.0 ppm
E: ± 10 ppm

Enable/Disable Function
B: Enable High (Pad 1)
S: Enable Low (Pad 1)
U: No Enable/Disable Function
G: Enable High (Pad 2)
M: Enable Low (Pad 2)

Output Type
F: No Voltage Control (TCXO)
V: Voltage Control (VCTCXO)

Output Waveform
P: LVPECL
L: LVDS
M: CML
C: CMOS

Package/Lead Configurations
N: Leadless Ceramic (9 Pad)
C: Leadless Ceramic (6 Pad)

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency Range	F_0	10 10		1400 135	MHz MHz	LVPECL, LVDS, CML [1] CMOS
Frequency Stabilities						
Initial Accuracy		-1.0		+1.0	ppm	@ +25°C
vs. Operating Temperature	$\Delta F/F$	See ordering information			ppm	(FMAX-FMIN)/2 [2]
vs. Supply Voltage			±0.40		ppm	5% voltage variation
vs. Reflow			±0.75		ppm	2 reflows max
vs. Supply Voltage			±0.20		ppm	5% load variation
vs. Aging		-3.0 -1.0		+3.0 +1.0	ppm Ppm	1st year Per year after 1st year
RF Output						
Output Load		50 Ω to (V_{CC} - 2) VDC 100 Ω Differential 15 pF				LVPECL [3] LVDS, CML [3] CMOS [3]
Symmetry (duty cycle)	T_{DC}	45 45 45		55 55 55	% % %	@ 50% of waveform (LVPECL) @ 1.25 V (LVDS) @ 50% V_{CC} (CMOS)
Logic "1" Level	V_{OH}	Vcc – 1.02 90% Vcc			V	CMOS Load
Logic "0" Level	V_{OL}			Vcc – 1.63 10% Vcc	V	CMOS Load
Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS
Differential Output Voltage		250	425	500	mV	LVDS Load
Common Mode Voltage			1.2		V	LVDS Output
Output Voltage Level		1.1	1.5	1.9	V_{pk-pk}	CML
Rise/Fall Time	T_R/T_F			0.35 6.0	ns ns	LVPECL, LVDS, CML CMOS
Start-up Time	T_{SU}			10	ms	
Frequency Adjustment						
Control Voltage Range	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.00	V V V	@ 1.8 V supply @ 2.5 V supply @ 3.3 V supply
Tuning Range		±5.0			ppm	VCTCXO only [4]
Linearity				10	%	
Input Impedance		500			kΩ	
Enable/Disable						
Enable/Disable Logic (Option B or G)		80% V_{CC}		 0.35	V V	Output Enabled Output disabled to HIGH Z
Enable/Disable Logic (Option S or M)		 80% V_{CC}		0.35	V V	Output Enabled Output disabled to HIGH Z

ELECTRICAL SPECIFICATIONS

Operating Voltage and Current						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	M6300
		2.375	2.500	2.625	V	M6301
		1.710	1.800	1.890	V	M6302
Operating Current	I_{CC}			125	mA	LVPECL
				100	mA	LVDS
				110	mA	CML
				90	mA	CMOS

Temperature						
Operating Temperature	T_A	See ordering information			°C	
Storage Temperature	T_S	-55		+125	°C	

Notes	
Note 1	Contact factory for frequencies over 945 MHz.
Note 2	Contact factory for less than ±1 ppm frequency stability.
Note 3	Refer to the load circuit diagram in this data sheet.
Note 4	Contact factory for other tuning range options.

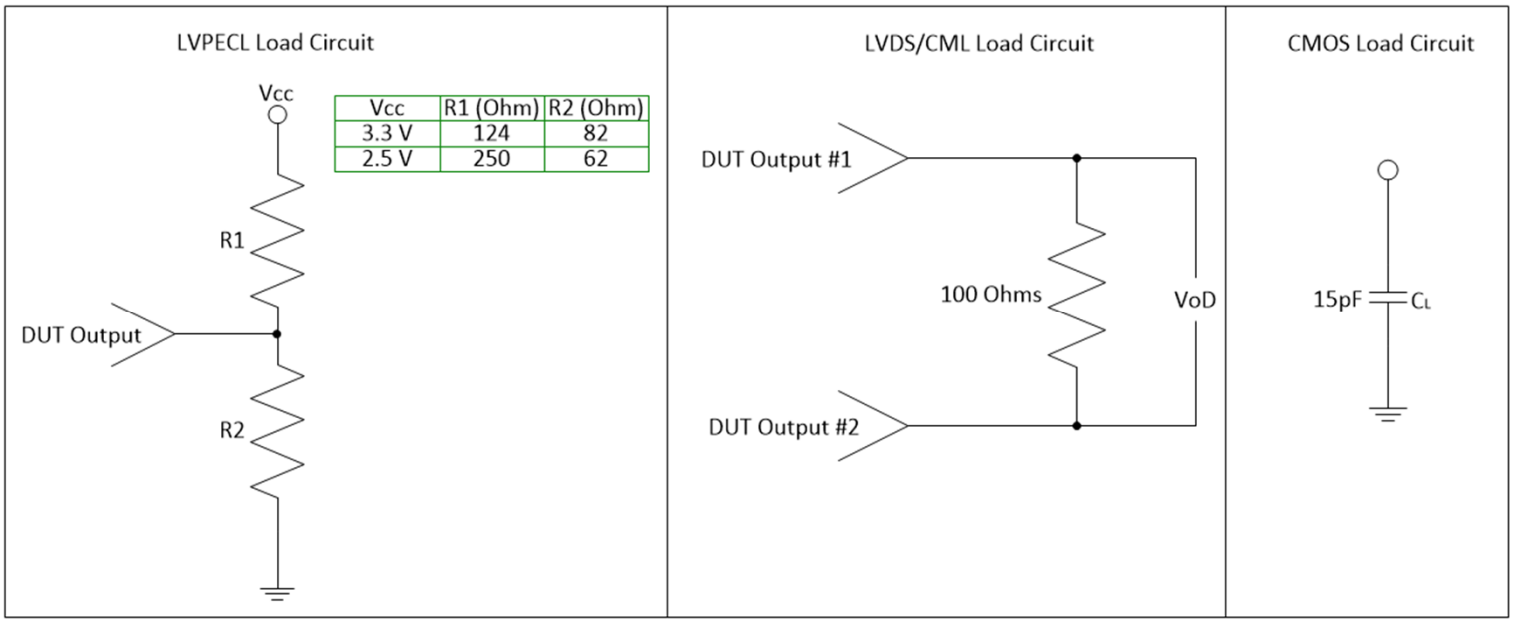
TEMPERATURE vs. STABILITY

	±0.5 ppm	±1.0 ppm	±2.0 ppm	±2.5 ppm	±4.6 ppm
0°C to +70°C	Available	Available	Available	Available	Available
-20°C to +70°C	Contact Factory	Available	Available	Available	Available
-40°C to +85°C	Contact Factory	Available	Available	Available	Available
-55°C to +105°C	Contact Factory	Contact Factory	Contact Factory	Contact Factory	Available
-55°C to +105°C	Contact Factory	Contact Factory	Contact Factory	Contact Factory	Available

ENVIRONMENTAL CONDITIONS

Shock	Per MIL-STD-202, Method 213, Condition C
Vibration	Per MIL-STD-202, Methods 201 & 204
Solderability	Per EIAJ-STD-002
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10-8 atm cc/s of helium)
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B

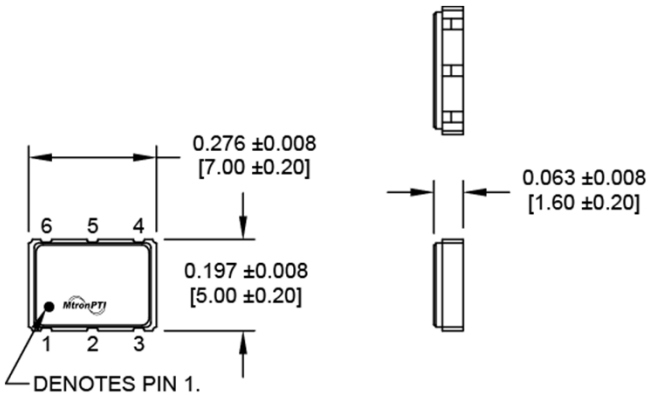
LOAD CIRCUIT DIAGRAMS

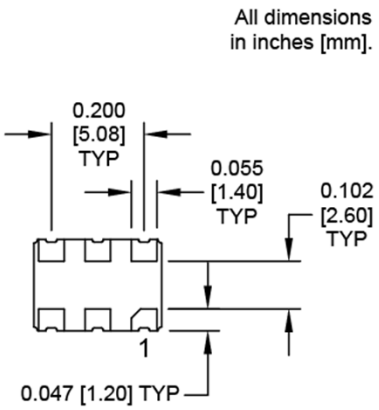


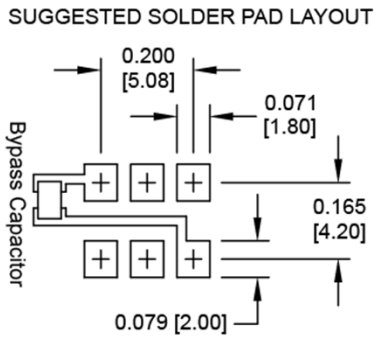
Vcc	R1 (Ohm)	R2 (Ohm)
3.3 V	124	82
2.5 V	250	62

MECHANICAL AND PIN OUT INFORMATION

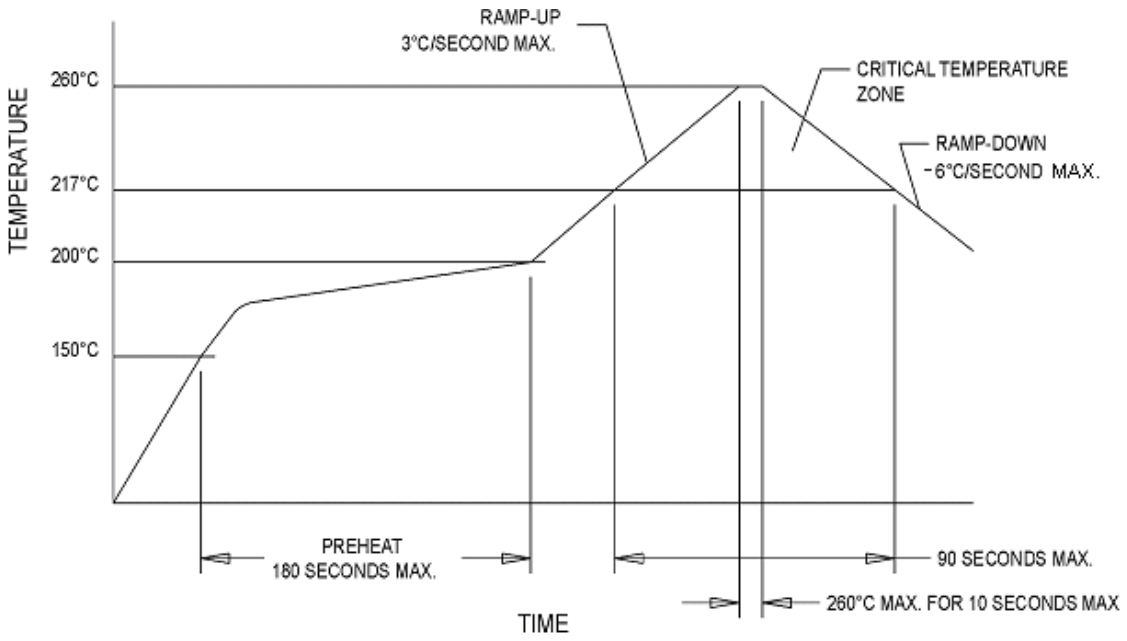
Pad	Function
1	Enable/Disable, Voltage Control or N/C
2	Enable/Disable, Voltage Control or N/C
3	Ground
4	Output Q (LVPECL, LVDS, CML, CMOS)
5	Output $\bar{Q}$ (LVPECL, LVDS, CML)
6	Supply Vcc+





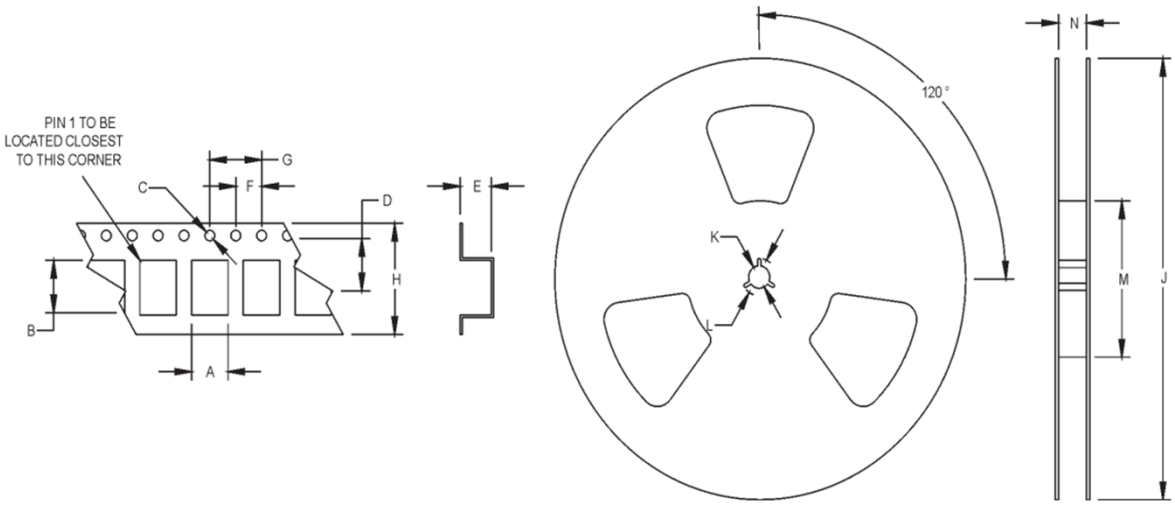


LEAD FREE SOLDER PROFILE



TAPE AND REEL SPECIFICATIONS

All units in mm



A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80