



PRODUCT / PROCESS CHANGE NOTIFICATION

Notification Date: 5/25/2006 Projected Completion Date:

PCN Number : **10113**

Product Identification (Including Customer P/N):

K1526B, K1526C, K1536B, K1536C products

Detailed Description of Changes:

The "B" and "C" configurations are being obsoleted (EOL). K1536B & K1536C are being replaced with the M3V series. The K1526C is being replaced by the K1526D. The K1526B is being replaced by the MVS series. See the attached data sheets for the K1526D and MVS for product specs.

Reason for Changes:

Due to low demand for this non-standard (9x11mm) package size, it is being obsoleted. It is being replaced with the industry standard 9x14mm package.

Projected Timing of Change and Implementation Date:

See below.

Anticipated Impact on Quality and Reliability:

None. Identical specifications for the EOL parts will not be supported by their replacements. See attached data sheets for the K1526D and MVS products.

Qualification Plan (if applicable):

Contact the factory

Last Time Buy Date:

July 31, 2006

Last Time Delivery Date and Comments (if applicable):

All product must be shipped no later than October 31, 2006.

Originated By: <u>Dick Thompson</u>	Date: <u>5/23/2006</u>
MtronPTI Engineering: <u>Joe Doyle</u>	Date: <u>5/24/2006</u>
MtronPTI Apps. Eng'r.: <u>Bill Jonnwein</u>	Date: <u>5/23/2006</u>
MtronPTI Sales or Designate: <u>Dick Thompson</u>	Date: <u>5/23/2006</u>
MtronPTI Operations: <u>Greg Anderson</u>	Date: <u>5/25/2006</u>
MtronPTI Quality Assurance: <u>JKocak</u>	Date: <u>5/24/2006</u>

CUSTOMER ACKNOWLEDGMENT:

This PCN will be considered acceptable and become effective on the date shown if no feedback is received within 30 days of notification denoted above.

PCN APPROVED:

Signature: _____

YES: [] NO: []

Title: _____ Date: _____

COMMENTS:

Please return this signed document to:

MtronPTI, 100 Douglas Ave., Yankton, SD, 57078 or email to pcn@mtronpti.com

K1526D Series

9x14 mm, 5.0 Volt, CMOS/TTL, VCXO



- Former **Champion Technologies, Inc.** Product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation

Ordering Information

00.0000 MHz

Product Series **K1526D** **X** **X**

Model Selection

A: ±100 - ±150 ppm Pull*

D: ±80 - ±130 ppm Pull*

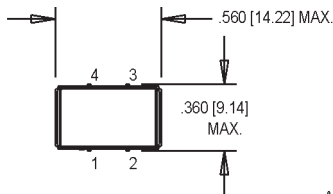
Temperature Range

Blank: 0°C to +70°C

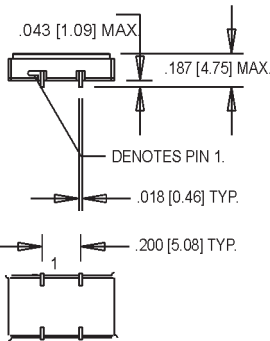
M: -40°C to +85°C

Frequency (customer specified)

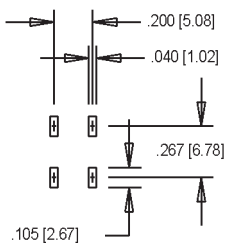
* Above 40 MHz, pull is ±100 ppm or ±80 ppm minimum (no maximum)



All dimensions in inches [mm].



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Voltage Control
2	Ground & Gnd Plane
3	Output
4	+Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	2		160	MHz		
Operating Temperature	T _A	(See ordering information)					
Storage Temperature	T _S	-40		+125	°C		
Frequency Stability Overall	ΔF/F	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
0°C to +70°C				±25	ppm		
-40°C to +85°C				±50	ppm		
Aging 1 st Year		-3/-5		+3/+5	ppm	< 52 MHz/ ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz/ ≥ 52 MHz	
Pullability/APR		(See ordering information)					
Control Voltage	V _c	0.5	2.5	4.5	V		
Linearity 2.000 to 33.000 MHz				5	%	Positive Monotonic Slope	
33.001 to 160.000 MHz				10	%		
Modulation Bandwidth	f _m	20			KHz	±3dB	
Input Impedance	Z _{in}	50k			Ohms	@ 10 kHz	
Input Voltage	V _{dd}	4.5	5.0	5.5	V		
Input Current	I _{dd}			26	mA		
Output Type						HCMOS/TTL	
Load		5 TTL or 15 pF HCMOS				See Note 1	
Symmetry (Duty Cycle) TTL & CMOS < 33 MHz		45		55	%	See Note 2	
CMOS ≥ 33 MHz		40		60	%		
Logic "1" Level	V _{oh}	4.5			V		
Logic "0" Level	V _{ol}			0.5	V		
Output Current				±16	mA		
Rise/Fall Time	T _r /T _f			4	ns		
Start up Time				10	ms		
Phase Jitter @ 26 MHz	φ _J		4		ps RMS	Integrated 12 kHz – 20 MHz	
Phase Noise (Typical) @ 26 MHz		100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier	
		-65	-95	-115	-130	-140	dBc/Hz

1. TTL load – see load circuit diagram #1 on page 116. HCMOS load – see load circuit diagram #2 on page 117.
2. Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with HCMOS load.

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Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

MVS Series

9x14 mm, 5.0 Volt, HCMOS/TTL, VCXO



- General purpose VCXO for Phase Lock Loops (PLL), Clock Recovery, Reference Signal Tracking and Synthesizers
- Frequencies up to 160 MHz and tri-state option

Ordering Information

00.0000
MHz

MVS 1 3 V 2 C J

Product Series _____

Temperature Range

1: 0°C to +70°C 2: -40°C to +85°C

6: -20°C to +70°C

Stability

1: ±1000 ppm 2: ±500 ppm

3: ±100 ppm 4: ±50 ppm

5: ±35 ppm 6: ±25 ppm

*8: ±20 ppm

Output Type

V: Voltage Controlled T: Tri-state

Pull Range (Vc = .5 to 4.5 V)

1: ±50 ppm min.

2: ±100 ppm min. (Up to 70.000 MHz)

Symmetry/Logic Compatibility

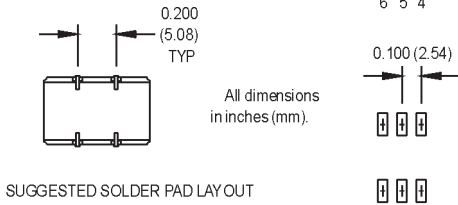
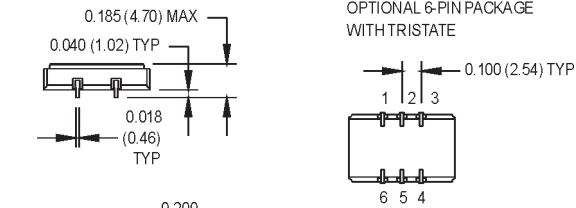
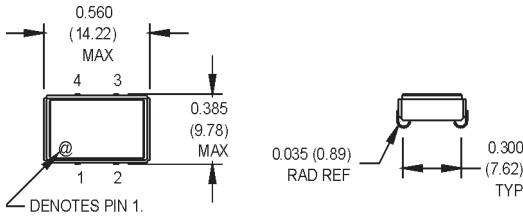
A: 40/60 CMOS/TTL C: 45/55 HCMOS

Package/Lead Configurations

J: J Lead

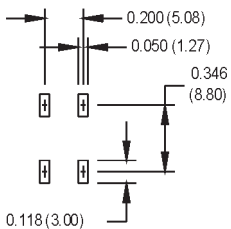
Frequency (customer specified) _____

*Contact factory for availability.



All dimensions in inches (mm).

SUGGESTED SOLDER PAD LAYOUT



Pin Connections

FUNCTION	4 Pin Pkg.	6 Pin Pkg.
Control Voltage	1	1
Tristate		2
Circuit/Case Ground	2	3
Output	3	4
N/C		5
+Vdd	4	6

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	1.544		160	MHz	See Note 1	
Operating Temperature	Ta	(See Ordering Information)					
Storage Temperature	Ts	-55		+125	°C		
Frequency Stability	ΔF/F	(See Ordering Information)					
Aging							
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz	
Pullability/APR		(See Ordering Information)					Over control voltage
Control Voltage	Vc	0.5	2.5	4.5	V		
Linearity				10	%	Positive Monotonic Slope	
Modulation Bandwidth	fm	10			kHz		
Input Impedance	Zin	50k			Ohms		
Input Voltage	Vdd	4.75	5.0	5.25	V		
Input Current	Idd		25	35	mA	1.544 to 24.999 MHz	
			35	60	mA	25 to 69.999 MHz	
			55	90	mA	70 to 160 MHz	
Output Type						HCMOS/TTL	
Load						See Note 2	
1.544 to 60 MHz		10 TTL or 50 pF					
60.001 to 160 MHz		5 TTL or 30 pF					
Symmetry (Duty Cycle)		(See Ordering Information)					See Note 3
Logic "1" Level	Voh	90% Vdd			V	HCMOS load	
		Vdd -0.5			V	TTL Load	
Logic "0" Level	Vol			10% Vdd	V	HCMOS load	
				0.5	V	TTL load	
Rise/Fall Time	Tr/Tf		3	10	ns	See Note 4	
Tristate Function		Input Logic "1" or floating: output active					
		Input Logic "0": output disables to high-Z					
Start up Time			4		ms		
Phase Jitter @ 155.52 MHz	φ J		10	15	ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical) @ 155.52 MHz		100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier	
		-62	-93	-113	-114	dBc/Hz	

1. Frequencies above 90 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies. Contact factory.
2. TTL load - see load circuit diagram #1 on page 116. HCMOS load - see load circuit diagram #2 on page 116.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

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