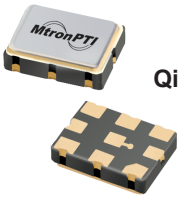
M21x Series Multiple Frequency Clock Oscillator

5.0 x 7.0 mm, 3.3/2.5/1.8 V, LVPECL/LVDS/CML/HCMOS Output

Product Features

- Multiple Output Frequencies (2, 3, or 4) - Selectable
- *QiK Chip™* Technology
- Superior Jitter Performance (less than 0.25 ps RMS, 12 kHz - 20 MHz)
- SAW replacement - better performance
- Frequencies from 50 MHz - 1.4 GHz (LVDS/LVPECL/CML)
- Frequencies from 10 MHz - 150 MHz (HCMOS)



Product Description

The multiple frequency oscillator utilizes MtronPTI's Qik Chip™ technology to provide a very low jitter clock for all output frequencies. The M21x is available with up to 4 different frequency outputs from 10MHz through 1.4 GHz. The M21x utilizes the stable fundamental 3rd overtone crystal and the Qik Chip™ IC to provide the wide range of output frequencies. Using this design approach, the M21x provides exceptional performance in frequency stability, jitter, phase noise and long term reliability.

Product Applications

- Global/Regional selection
- Forward Error Correction (FEC) / Selectable Functionality applications
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- 1-2-4-10 Gigabit Fibre Channel
- Wireless base stations / WLAN / Gigabit Ethernet
- xDSL, Network Communications
- Avionic flight controls
- Military communications
- Clock and data recovery
- Low jitter clock generation
- Frequency margining

Product Ordering Information

Ordering Information

M21 x x x x x x x x -SXXX

Product Series

Number of Frequencies
- **2:** Two Selectable Frequencies
- **3:** Three Selectable Frequencies
- **4:** Four Selectable Frequencies

Supply Voltage
- **0:** 3.3 V
- **1:** 2.5 V
- **2:** 1.8 V

Operating Temperature
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C

Stability
- **4:** ±50 ppm **3:** ±100 ppm
- **8:** ±20 ppm

Enable/Disable Function
- **B:** Enable High (Pad 1) **G:** Enable High (Pad 2)
- **S:** Enable Low (Pad 1) **M:** Enable Low (Pad 2)

Logic Type
- **P:** LVPECL **L:** LVDS
- **M:** CML **C:** HCMOS

Two Frequency Select Function
- **1:** FS0=Pad 1
- **2:** FS0=Pad 2
- ***A:** FS0=Pad A

Package/Lead Configuration
- **N:** 5 x 7 mm Leadless

Factory Assigned to Accommodate

Customer Specified Frequencies - Contact Factory

***For three and four frequency selections, FS0=Pad A**

M2120Sxxx, M2121Sxxx, M2122Sxxx, M2130Sxxx, M2131Sxxx, M2132Sxxx, M2140Sxxx, M2141Sxxx, M2142Sxxx - Contact factory for datasheets.

Frequency Select Truth Table		
	FS1	**FS0**
Frequency 1	High	High
Frequency 2	High	Low
Frequency 3	Low	High
Frequency 4	Low	Low

NOTE: Logic Low = 20% Vcc max.
Logic High = 80% Vcc min.

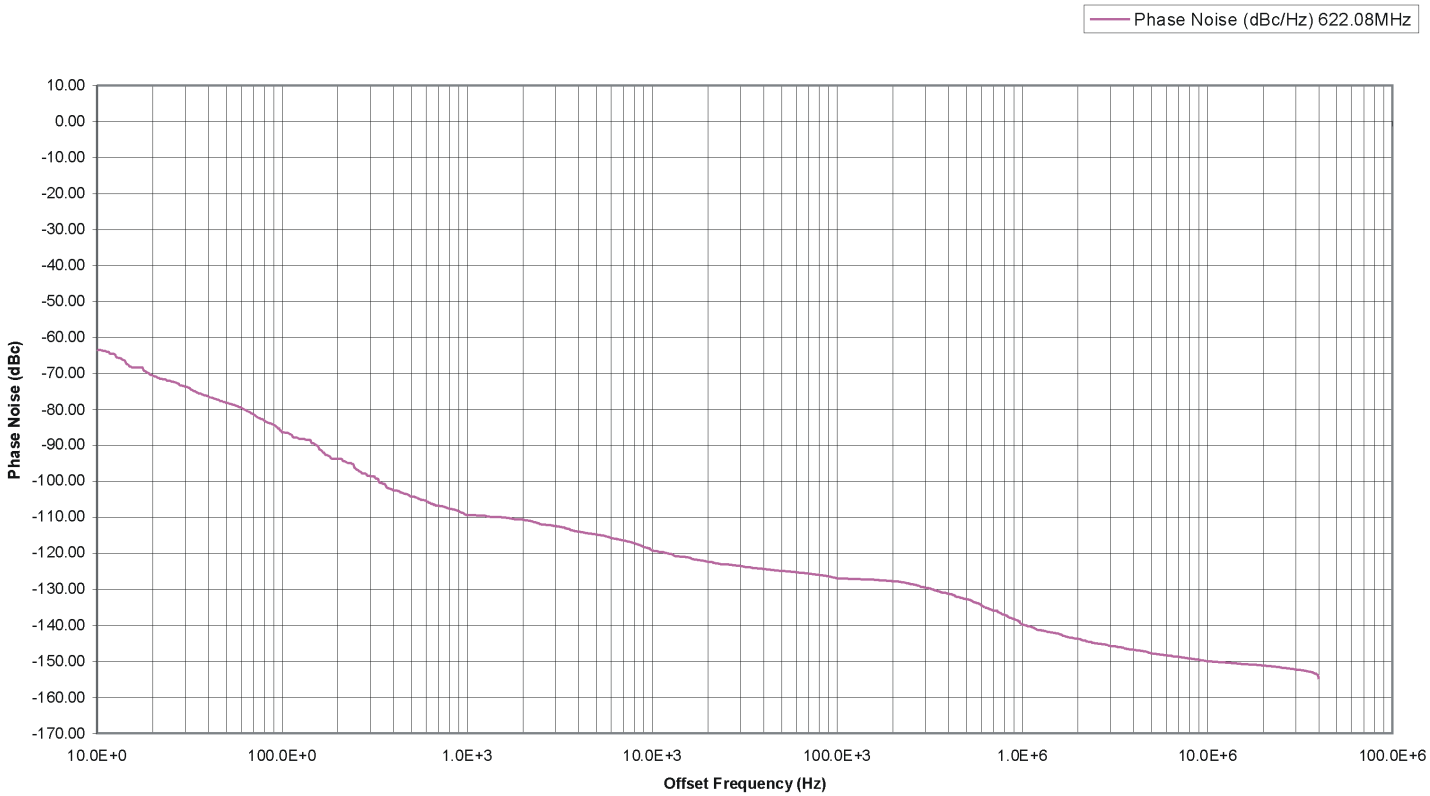
Rev: 08/16/2013

Performance Characteristics

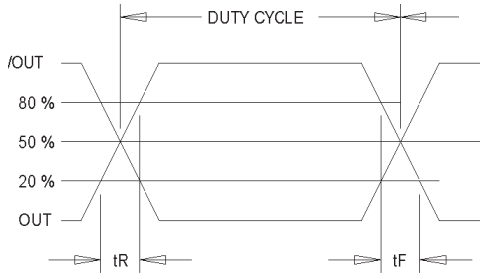
	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Electrical Specifications	Frequency Range	F	50 10		1400 150	MHz	LVPECL/LVDS/CML - See Note 1 HCMOS
	Operating Temperature	TA	-20 to +70 -40 to +85			°C °C	Customer Specified
	Storage Temperature	TS	-55		+125	°C	
	Frequency Stability	ΔF/F	See Ordering Information			ppm	See Note 2
	Aging 1st Year Thereafter (per year)		 -3 -1		 +3 +1	 ppm ppm	
	Supply Voltage	Vcc	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V V V	
	Input Current	Icc			125 105	mA mA	LVPECL/HCMOS/CML LVDS
	Load		 50 Ohms to (Vcc –2) Vdc 100 Ohm differential load 		 15	 pF	See Note 3 LVPECL Waveform LVDS/CML Waveform CMOS Waveform
	Symmetry (Duty Cycle)		45		55	%	LDPECL: Vdd – 1.3 V LVDS: 1.25 V
	Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS
	Differential Voltage	Vod	250	350	450	mV	LVDS
		Vod	0.7	0.95	1.20	Vpp	CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc -1.02			V	LVPECL
			90% Vdd				HCMOS
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
					10% Vdd		HCMOS
	Rise/Fall Time	Tr/Tf		0.23	0.35	ns	@ 20/80% LVPECL, LVDS, CML
					6.0	ns	Ref. 10%-90% Vdd HCMOS
	Enable Function Option B		80% Vcc min. or N/C: Output active 0.5V max: Output disables to high-Z				Customer Specified
	Enable Function Option S		0.5V max or N/C: Output active 80% Vcc min: Output disables to high-Z				Customer Specified
	Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z				Customer Specified
	Frequency Selection		See Truth Table				
	Settling Time				10	ms	To within ± 1 ppm of frequency
	Start up Time				10	ms	
	Phase Jitter						
	@ 622.08 MHz	ϕJ		0.25		ps RMS	LVPECL/LVDS/CML Integrated 12 kHz – 20 MHz
	@ 125 MHz				0.50	ps RMS	HCMOS (12 kHz – 20 MHz)
Environmental							
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)					
	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
	Hermeticity	Per MIL-STD-202, Method 112, ($1x10^{-8}$ atm. cc/s of Helium)					
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)					
	Solderability	Per EIAJ-STD-002					
	Max. Soldering Cond.	See solder profile, Figure 1					

Note 1: Contact factory for standard frequency availability over 945 MHz.
Note 2: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 3: See Load Circuit Diagram in this datasheet. Consult factory with nonstandard output load requirements.

Phase Noise Plot

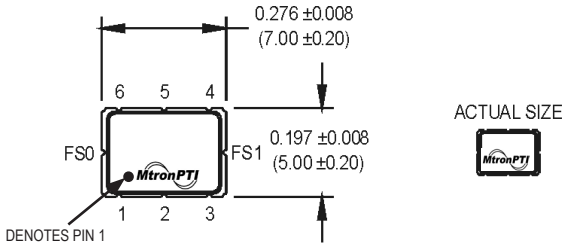


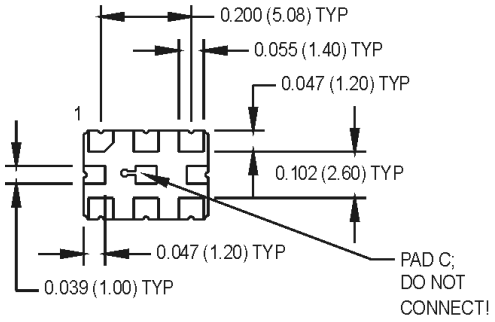
Output Waveform



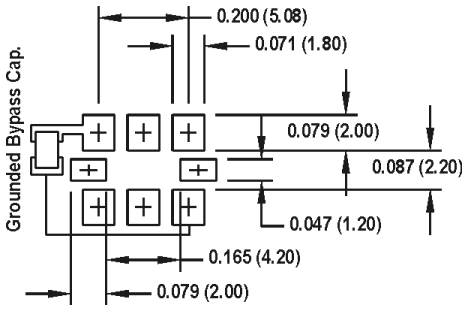
Output Waveform: LVDS/CML/LVPECL

Product Dimension & Pinout Information





SUGGESTED SOLDER PAD LAYOUT



PAD 1 ENABLE
Pad1: Enable/Disable or Tristate
Pad2: N/C or FS0
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML,HCMOS)
Pad5: Output $\overline{Q}$ (LVPECL,LVDS,CML) N/C for HCMOS
Pad6: Vcc
PadA: FS0 or N/C
PadB: FS1
PadC: Do not connect!

PAD 2 ENABLE
Pad1: N/C or FS0
Pad2: Enable/Disable or Tristate
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML,HCMOS)
Pad5: Output $\overline{Q}$ (LVPECL,LVDS,CML) N/C for HCMOS
Pad6: Vcc
PadA: FS0 or N/C
PadB: FS1
PadC: Do not connect!

Handling Information

Although protection circuitry has been designed into the M21x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Model	ESD Threshold, Minimum	Unit
Human Body	1500*	V
Charged Device	1500*	V

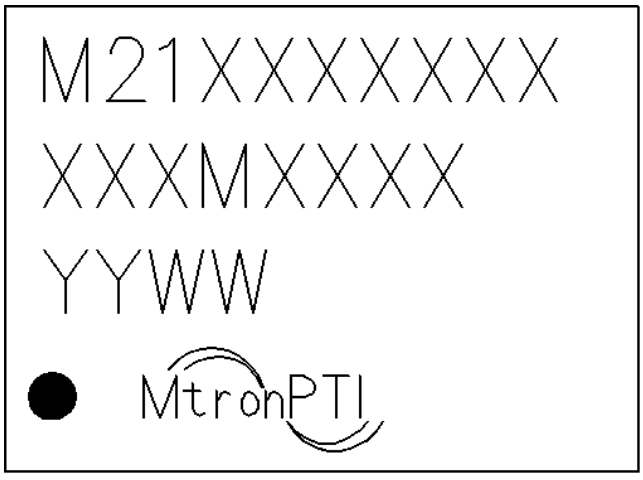
* MIL-STD-833D, Method 3015, Class 1

Quality Parameters

Environmental Specifications/Qualification Testing Performed on the M21x Clock Oscillator		
Test	**Test Method**	**Test Condition**
Electrical Characteristics	Internal Specification	Per Specification
Frequency vs. Temperature	Internal Specification	Per Specification
Mechanical Shock	MIL-STD-202, Method 213, C	100 g's
Vibration	MIL-STD-202, Method 201-204	10 g's from 10-2000 Hz
Thermal Cycle	MIL-STD-883, Method 1010, B	-55 Deg. C to +125 Deg. C, 15 minute Dwell, 10 cycles
Aging	Internal Specification	168 Hours at 105 Degrees C
Gross Leak	MIL-STD-202, Method 112	30 Second Immersion
Fine Leak	MIL-STD-202, Method 112	Must meet $1x10^{-8}$
Solderability	MIL-STD-883, Method 2003	8 Hour Steam Age – Must Exhibit 95% coverage
Resistance to Solvents	MIL-STD-883, Method 2015	Three 1 minute soaks
Terminal Pull	MIL-STD-883, Method 2004, A	2 Pounds
Lead Bend	MIL-STD-883, Method 2004, B1	1 Bending Cycle
Physical Dimensions	MIL-STD-883, Method 2016	Per Specification
Internal Visual	Internal Specification	Per Internal Specification

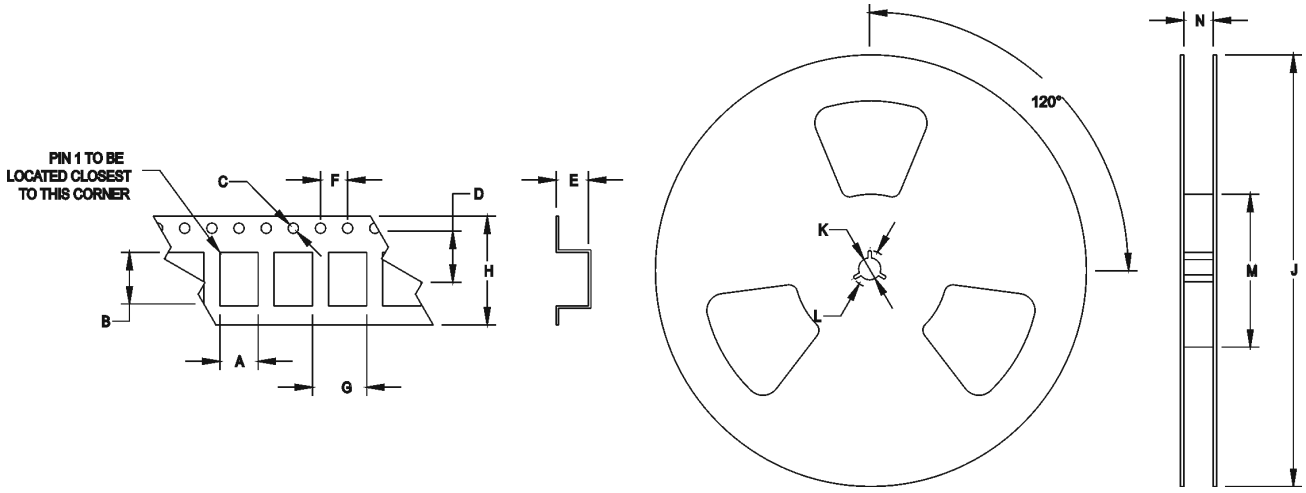
Part Marking Guide

Line 1: Model Number
Line 2: Frequency
Line 3: Date Code
Line 4: Pin 1 Indicator / MtronPTI



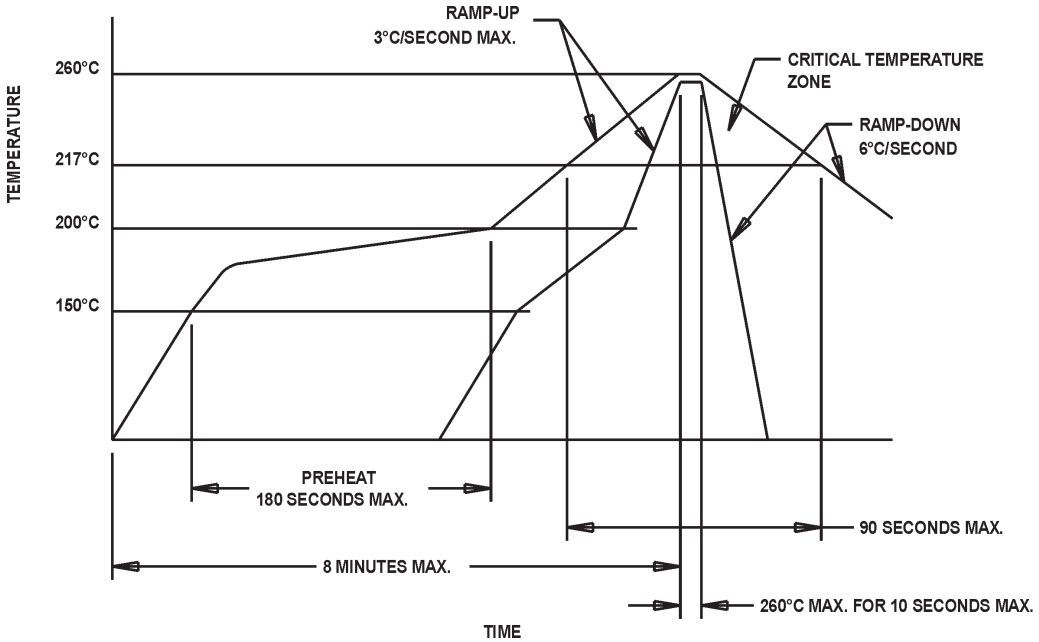
Tape & Reel Specifications

(all measurements are in mm)	A	B	C	D	E	F	G	H	I	J	K	L
M21x	6.51	9.29	1.5	7.5	2.8	4	8/12	16	180-330	13	21	60-100



Standard Tape and Reel: 1000 parts per reel

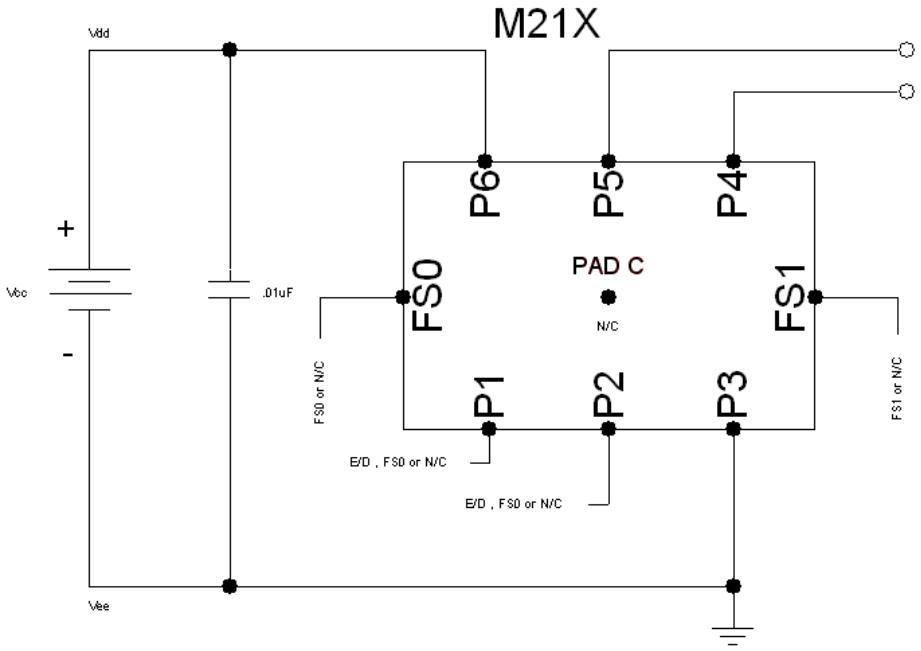
Maximum Soldering Conditions

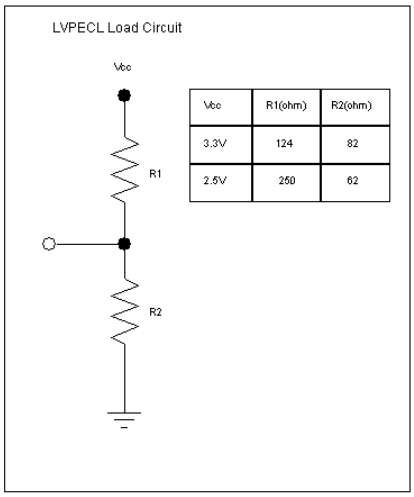


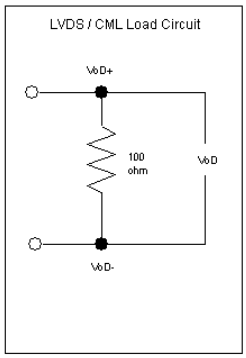
Solder Conditions

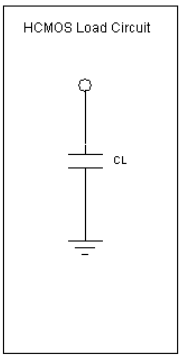
Note: Exceeding these limits may damage the device.

Typical Test Circuit & Load Circuit Diagrams









Product Revision Table

Date	Revision	PCN Number	Details of Revision
7/20/07	A	10118	IC Revision to improve phase noise and electrical performance

For custom products or additional specifications contact our sales team at
800.762.8800 (toll free) or 605.665.9321

For more information on this product visit the MtronPTI website at
www.mtronpti.com