



## M2065/2066 Ultra Low Jitter Oscillators 3.2x2.5mm ceramic package

**MtronPTI** has introduced a new family of high-performance crystal oscillators – M2065/2066. Offering the industry's lowest jitter solution, the M2065/2066 family of oscillators can deliver performance to less than 100 femtoseconds (fs) RMS jitter in a small 3.2x2.5mm ceramic package.

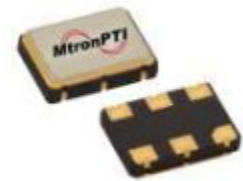
The growing demand for network bandwidth and faster data rates continue to drive the need for lower jitter reference clocks. High clock jitter can cause high bit error rates, lost traffic or the loss of system communication. Using an ultra low jitter clock can eliminate these performance risks. The M2065/2066 family of oscillators provide best-in-class frequency stability and superior jitter performance to meet these demanding applications.

### Features:

- Ultra Low Jitter <100fs RMS Jitter (12kHz-20MHz @156.25MHz )
- Standard 3.2x2.5mm ceramic package
- Industrial Temp range -40 °C to +85 °C
- LVPECL / LVDS output

### Applications:

- Datacenter
- Optical Module
- Military Communications
- Broadcast Video



Output Type
Parameter
Frequency of Operation
Frequency Stability
Aging
Output Type
Output Load
Symmetry (duty cycle)
Logic Level "1"
Logic Level "0"
Rise/Fall Time
Start-up Time
Enable Logic
Disable Logic
Operating Voltage
Supply Current
Operating Temperature Range
Phase Jitter (RMS)

LVPECL OUT PUT						
Symbol	Min.	Typ.	Max.	Units	Conditions	
F <sub>O</sub>	25		220	MHz		
Frequency Stability						
ΔF/F	+/-20ppm				Other stability options available	
Aging	-5		5	ppm	1 <sup>st</sup> year	
RF Output						
LVPECL Compatible						
Output Load	50 Ω to (V <sub>cc</sub> -2.0) VDC			V		
Symmetry (duty cycle)	V <sub>OH</sub>	45	55	%	Ref. to 50% of waveform	
Logic Level "1"	V <sub>OH</sub>	V <sub>cc</sub> -1.025	V <sub>cc</sub> -0.880	V		
Logic Level "0"	T <sub>DC</sub>	V <sub>cc</sub> -1.810	V <sub>cc</sub> -1.620	V		
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	0.2	0.4	ns	20% to 80% of waveform	
Start-up Time	T <sub>SU</sub>		10	ms	T <sub>ambient</sub> = +25°C	
Enable Logic		70% V <sub>cc</sub> or N/C		V	Pad 1 or Pad 2: Output Enabled	
Disable Logic			30% V <sub>cc</sub>	V	Pad 1 or Pad 2: Output Disabled to high-Z	
Supply Voltage & Power Consumption						
Operating Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	2.5V option available
Supply Current	I <sub>cc</sub>			75	mA	
Other Parameters						
	-40 °C to +85 °C				Other temp options available	
Phase Jitter (RMS)	Φ <sub>J</sub>		0.1	ps	12 KHz to 20 MHz 156.25 MHz	

LVDS OUTPUT						
Symbol	Min.	Typ.	Max.	Units	Conditions	
F <sub>O</sub>	25		220	MHz		
Frequency Stability						
ΔF/F	+/-20ppm				Other stability options available	
Aging	-5		5	ppm	1 <sup>st</sup> year	
RF Output						
LVDS Compatible						
Output Load	100 Ω Differential			V		
Symmetry (duty cycle)	V <sub>OH</sub>	45	55	%	Ref. to 50% of waveform	
Logic Level "1"	V <sub>DIFF</sub>	250	350	450	mV	peak-to-peak differential output voltage
Logic Level "0"	V <sub>OS</sub>	1.125	1.25	1.375	V	
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	0.2	0.4	ns	20% to 80% of waveform	
Start-up Time	T <sub>SU</sub>		10	ms	T <sub>ambient</sub> = +25°C	
Enable Logic		70% V <sub>cc</sub> or N/C		V	Pad 1 or Pad 2: Output Enabled	
Disable Logic			30% V <sub>cc</sub>	V	Pad 1 or Pad 2: Output Disabled to high-Z	
Supply Voltage & Power Consumption						
Operating Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	2.5V option available
Supply Current	I <sub>cc</sub>			40	mA	
Other Parameters						
	-40 °C to +85 °C				Other temp options available	
Phase Jitter (RMS)	Φ <sub>J</sub>		0.15	ps	12 KHz to 20 MHz 156.25 MHz	

