1703 E. Highway 50 Yankton, SD 57078 USA
Phone: 800-762-8800 or 605-665-9321 Fax: 605-665-1709
Website: www.mtronpti.com

SPECIFICATION FOR SMT VCTCXO
MtronPTI P/N: M6054S021

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O		24.000000		MHz	
Frequency Stability						
Frequency Tolerance		-2.0		+2.0		@ +25°C initial, Vc = 1.50
Frequency Stability ([max.-min.]/2)	ΔF/F	-0.28		+0.28	ppm	Operating Temperature Range 0 to +70 °C
		-1.5		+1.5	ppm	Operating Temperature Range -40 to +85 °C
Aging	$\Delta F_{AGE}/F$	-1.0		+1.0	ppm	1st year
Frequency Vs. Supply	$\Delta F_{VDD}/F$			±0.3	ppm	For ±5% voltage change
Frequency Vs. Output Load	$\Delta F_{LOAD}/F$			±0.2	ppm	For ±10% load change
Output						
Output Type		CMOS Compatible				
Output Load			15		pF	
Symmetry (duty cycle)	T_{DC}	45	50	55	%	@ 50% of V_{DD}
Logic "1" Level	V_{OH}	90% Vdd			% V_{DD}	CMOS load
Logic "0" Level	V_{OL}			10% Vdd	V	CMOS load
Rise/Fall Time	T_R/T_F			5	ns	From 10% to 90% Vdd
Startup Time	T_{SU}			2	ms	
Voltage Tuning						
Tuning Voltage		0.50	1.50	2.50	V	Pad 1
Tuning Range		±5			ppm	Ref. to frequency with Vc=1.50
Input Impedance	Z_{IN}	100			KΩ	
Supply Voltage & Power Consumption						
Operating Voltage	V_{DD}	3.135	3.30	3.465	V	
Operating Current	I_{DD}			6	mA	

Environmental Conditions:

Operating Temperature	T_A	-40		+85	°C	
Storage Temperature	T_S	-40		+85	°C	
Mechanical Shock	Per MIL-STD-202, Method 213 (2000 g, 0.3 ms duration, ½ sine wave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Hermeticity	Per MIL-STD-202, Method 112 (1x10-8 atm.cc/s of helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1					
Package Type	5.0 x 3.2 x 1.55 mm, Ceramic Leadless Chip Carrier (M6054 Series)					

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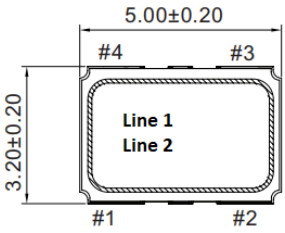
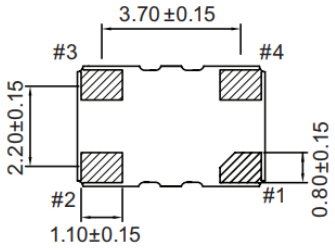
Mechanical, Marking and Layout Information:

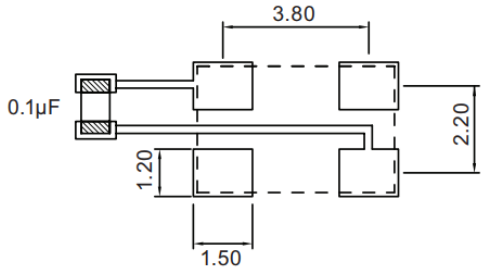
Part Marking	
Line 1	24M000
Line 2	M yy ww vv

Legend	
yy	Last 2 digits of year
ww	Week number
vv	Factory Code

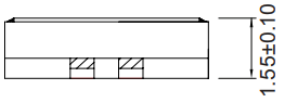
Pad	Function
1	Tuning Voltage
2	GND
3	Output
4	$+V_{DD}$







For optimal performance,
place a 0.1uF bypass capacitor
as close to Vdd and GND as possible



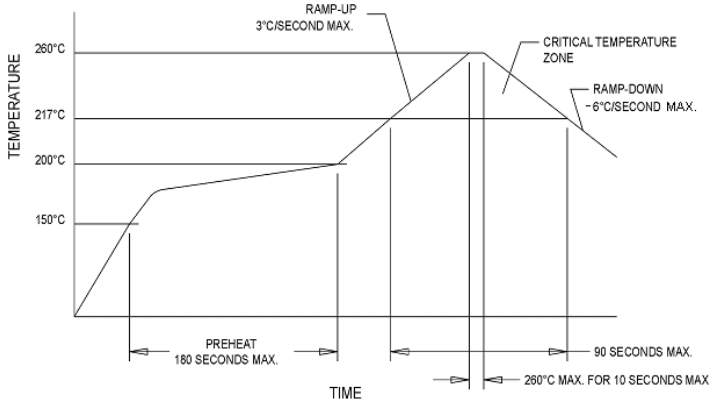


Figure 1

Datasheet Revision Table:

Date	Rev.	Author	Details of Revision
02/12/18	0	MM	Original Release.
08/01/18	A	DCO	Revised stability spec; revised marking to 2 digit factory code.