



SPECIFICATION FOR SMT VCTCXO

MtronPTI P/N: M6054S022

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F _O		10.000000		MHz	
Frequency Stability						
Frequency Stability	ΔF/F	-0.5		+0.5	ppm	Over -40°C to +85°C range. (Relative to frequency @+25°C)
Aging	ΔF _{AGE} /F	-0.5		+0.5	ppm	Per year
Frequency Vs. Supply	ΔF _{VDD} /F			±0.2	ppm	For ±5% voltage change
Frequency Vs. Output Load	ΔF _{LOAD} /F			±0.2	ppm	For ±10% load change
Output						
Output Type		CMOS Compatible				
Output Load			15		pF	
Symmetry (duty cycle)	TDC	45	50	55	%	@ 50% of VDD
Logic "1" Level	V _{OH}	90% V _{DD}			% V _{DD}	CMOS load
Logic "0" Level	V _{OL}			10% V _{DD}	V	CMOS load
Output Current Levels	I _{OH}			+4	mA	90% V _{DD} Min
	I _{OL}			-4	mA	10% V _{DD} Max
Rise/Fall Time	T _R /T _F			6	ns	From 10% to 90% V _{DD}
Startup Time	T _{SU}			2	ms	
Voltage Tuning						
Tuning Slope		Positive				
Tuning Voltage		0.50	1.50	2.50	V	Pad 1
Tuning Range		±5			ppm	Ref. to frequency with V _c =1.50
Input Impedance	Z _{IN}	100			KΩ	
Additional Specifications						
Phase Noise (Under Static Conditions)			-91		dBc/Hz	@ 10 Hz
			-117			@ 100 Hz
			-139			@ 1 kHz
			-153			@ 10 kHz
			-157			@ 100 kHz
Period Jitter	PJ		2.5		ps	RMS
			21		ps	Peak to Peak
Supply Voltage & Power Consumption						
Operating Voltage	V _{DD}	2.97	3.30	3.63	V	
Operating Current	I _{DD}			3.5	mA	

Environmental Conditions:

Operating Temperature	T _A	-40		+85	°C	
Storage Temperature	T _S	-55		+125	°C	
Mechanical Shock	Per MIL-STD-202, Method 213 (2000 g, 0.3 ms duration, ½ sine wave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Hermeticity	Per MIL-STD-202, Method 112 (1x10 ⁻⁸ atm.cc/s of helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1					
Package Type	5.0 x 3.2 x 1.55 mm, Ceramic Leadless Chip Carrier (M6054 Series)					

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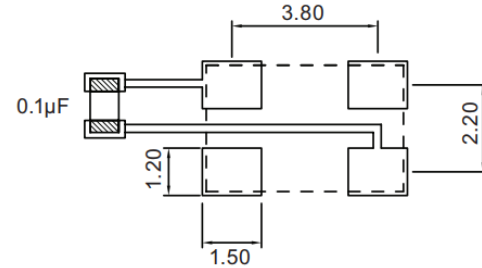
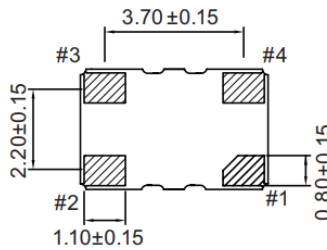
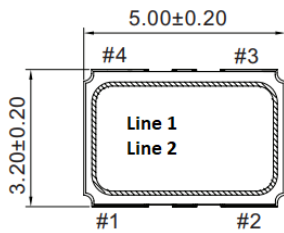
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Mechanical, Marking and Layout Information:

Part Marking	
Line 1	10M000
Line 2	M yy ww vv

Legend	
yy	Last 2 digits of year
ww	Week number
vv	Factory Code

Pad	Function
1	Tuning Voltage
2	GND
3	Output
4	+V _{DD}



For optimal performance, place a 0.1µF bypass capacitor as close to V_{DD} and GND as possible

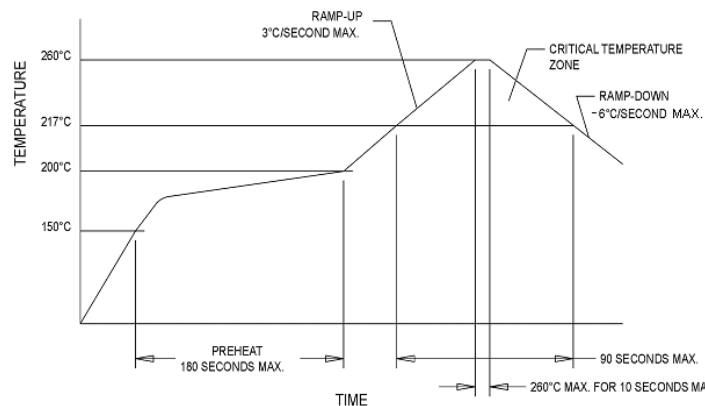
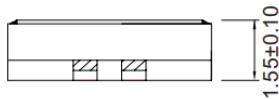


Figure 1

Datasheet Revision Table:

Date	Rev.	Author	Details of Revision
02/26/18	0	MM	Original Release.