1703 E. Highway 50 Yankton, SD 57078 USA
Phone: 800-762-8800 or 605-665-9321 Fax: 605-665-1709
Website: www.mtronpti.com

SPECIFICATION FOR SMT VCTCXO
MtronPTI Part Number M6056S010

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency	F_O		26.000000		MHz	
Frequency Tolerance		-1.0		+1.0	ppm	@ +25°C, Vc = 1.65V
Frequency Stability (ref. to +25 °C)	ΔF/F	-1.0		+1.0	ppm	-40 to +85 °C
Freq. v. Temp. Slope				1.0	ppm/°C	Measured every 2 °C or smaller increments
Freq. v. Temp. Hysteresis				0.6	ppm	Measured @ +25 °C
Frequency Change Through Reflow Soldering	ΔF/F	-1.0		+1.0	ppm	from before to after 2 reflow profiles, +260C peak for 10s
Frequency Vs. Load		-0.2		+0.2	ppm	For 10% load change
Frequency Vs. Supply		-0.1		+0.1	ppm	For 5% voltage change
Frequency Vs. Aging		-1.0		+1.0	ppm	Per year @ 25°C, ±2°C
Operating Temperature	T_A	-40		+85	°C	
Operating Voltage	V_{DD}	2.4	3.0	3.3	V	
Operating Current	I_{DD}			2.0	mA	
Output Type			Clipped Sine Wave			
Output Load			9 to 11 KΩ || 9 to 11 pF			
Output Level		0.8			V_{pk-pk}	DC-cut output capacitor required.
Control Voltage Range	V_C	0.50	1.65	2.80		Pad 1
Tuning Range		±6		±15	ppm	Pad 1
Control Voltage Input Impedance		500			KΩ	
Tuning Linearity				20%		
Phase Noise			-55		dBc/Hz	@ 1 Hz
			-85		dBc/Hz	@ 10 Hz
			-108		dBc/Hz	@ 100 Hz
			-130		dBc/Hz	@ 1 kHz
			-145		dBc/Hz	@ 10 kHz

Environmental Conditions:

Mechanical Shock	100 g's, 11 ms duration, half sine wave
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 20-2000 Hz)
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)
Storage Temperature	-40°C to +85°C
Solderability	Per EIAJ-STD-002
Max. Soldering Conditions	See solder profile, Figure 1
Package	4-pad 2.5 X 3.2 X 1.1 mm leadless ceramic. RoHS compliant.

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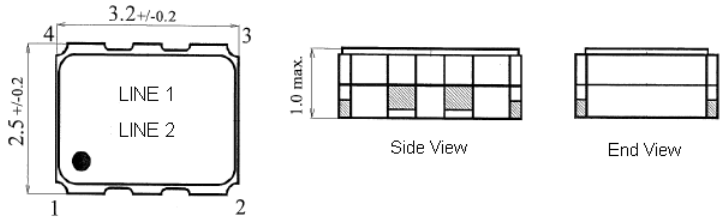
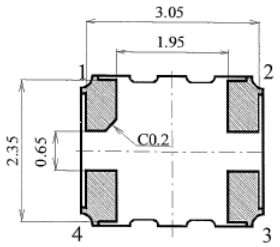
Dimensions, Marking, and Pin Out Information:

Part Marking	
Line 1	26M00
Line 2	M y w v

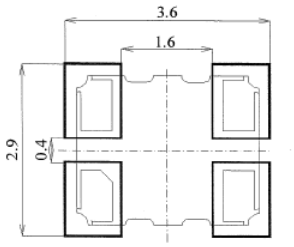
Legend	
y	Year
w	Work Week
v	Factory Code

Pin	Function
1	Control Voltage
2	Ground
3	Output
4	$+V_{DD}$



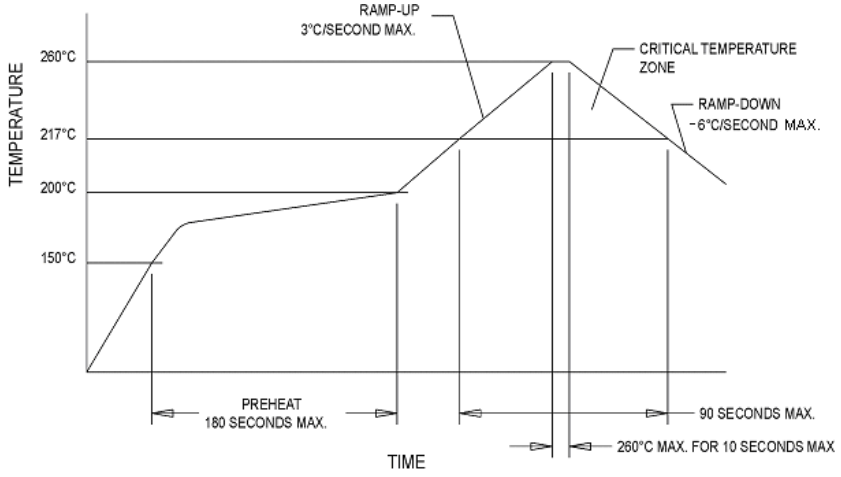


All dimensions are in mm.



Suggested Land Pattern (Top View)

A power supply bypass capacitor of value 0.01 µF or greater should be placed between $+V_{dd}$ and ground, near the device.



DATA SHEET REVISION TABLE:

Date	Rev.	Author	Details of Revision
04/25/16	0	DPD	Original release