UVC Series

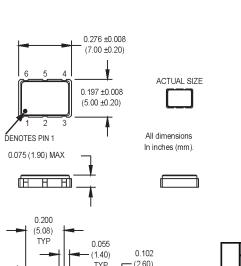
5x7 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillators

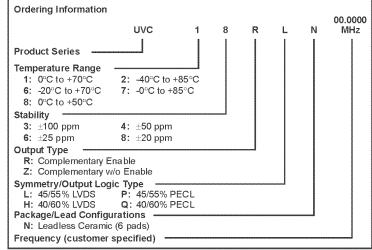








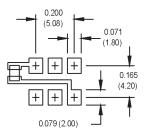




M2022Sxxx - Contact factory for datasheet.

0.200 (5.08) TYP 0.055 (1.40) TYP 0.047 (1.20) TYP	0.102 (2.60) TYP

SUGGESTED SOLDER PAD LAYOUT



Pad Connections

Pad	Function
1	Enable/Disable for "R" Output Type or N/C for "Z" Output Type
2	N/C
3	Ground
4	Output Q
5	Complementary Output Q
6	+ Vdd

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes		
	Freguency Range	F	0.75	. , , , .	800	MHz			
	Operating Temperature	TA	2 11 2	ee orderi	ng information	*****			
	Storage Temperature	Ts	-55		+125	ľ∘c			
	Frequency Stability	ΔF/F	(S	ee orderi	ng information		See Note 1		
	Aging	ney stability Airi (See ord							
	1st Year		-3		+3	ppm			
	Thereafter (per year)		-1		+1	ppm			
	Input Voltage	Vcc	3.135	3.3	3.465	٧			
	PECL Input Current	lcc			70	mA	0.75 to 24 MHz		
S			l		100	mΑ	24 to 96 MHz		
Į₽					110	mA	96 to 800 MHz		
ca	LVDS Input Current	lcc	l		30 60	mA	0.75 to 24 MHz 24 to 96 MHz		
1 ≒			l		60	mA mA	96 to 800 MHz		
Electrical Specifications	Output Type				00	IIIA	PECL/LVDS		
1 8	Load						See Note 2		
1,2	Load		5)	PECL Waveform				
듗				00 Ohm o		LVDS Waveform			
Ĭ	Symmetry (Duty Cycle)		(S	ee orderi	ng informatior	n)	@ 50% of waveform		
	Output Skew		<u> </u>		200	ps	PECL		
	Differential Voltage	Vod	250	350	450	mV	LVDS		
	Logic "1" Level	Voh	Vcc -1.02			٧	PECL		
	Logic "0" Level	Vol			Vcc -1.63	٧	PECL		
	Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL		
ш				0.50	1.0	ns	@ 20/80% LVDS		
	Enable Function		80% Vcc min or N/C: output active 20% Vcc max: output disables to high-Z				Output Option R		
			20% Vcc m	ax: outpu	7				
	Start up Time				10	ms			
	Phase Jitter (Typical)	φЈ		3	5	ps RMS	Integrated 12 kHz – 20 MHz		
豆									
en	Mechanical Shock MIL-STD-202, Method 213, C (100 g's)								
E									
2. □									
2	Hermeticity	MIL-STD-202, Method 112							
Ι"	Solderability	Per EIAJ-STD-002							
	Max Soldering Conditions See solder profile, Figure 1								

- 1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage and aging.
- 2. PECL load see Load Circuit Diagram #5. LVDS load see load circuit diagram #9.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.





